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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PATEL, KAUSHIKKUMAR M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,428	KIRSCH, GRAHAM	
	Examiner	Art Unit	
	Kaushikkumar Patel	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,19,32,33 and 52* is/are rejected.

7)☒ Claim(s) *3-18,20-31,34-51 and 53-65* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on January 16, 2004 have considered by the examiner.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to

be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1 - 2, 19, 32 - 33, and 52 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 - 2, 19, 33 of copending Application No. 10/629,378. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claimed subject matter of the instant application is equivalent to the claimed subject of the copending application.

4. As per claim 1:

An integrated circuit active memory device fabricated on a single semiconductor substrate, the active memory device comprising:

a memory device having a data bus containing a plurality of data bus bits (Claim 1 lines 2 - 3);

an array of processing elements with each processing element coupled to a respective group of the data bus bits, each of the processing elements having an instruction input coupled to receive processing element instructions for controlling the operation of the processing elements (Claim 1 lines 4 - 7);

an array control unit coupled to the processing elements in the array, the array control unit being operable to generate and to couple respective sets of the processing

element instructions to the processing elements responsive to each of a plurality of array control unit commands applied to a command input of the array control unit (Claim 1 lines 8 – 10);

a memory device control unit coupled to the memory device, the memory device control unit being operable to generate and to couple respective sets of memory commands to the memory device responsive to each of a plurality of memory device control unit commands applied to a command input of the memory device control unit (Claim 1 lines 11 – 15); and

a command engine coupled to the array control unit and the memory device control unit, the command engine being operable to couple to the array control unit respective sets of the array control unit commands and to couple to the memory device control unit respective sets of the memory device control unit commands responsive to respective task commands applied to a task command input of the command engine (Claim 1 lines 16 - 21).

As per claim 2:

The memory device comprises a dynamic random access memory device (Claim 2.)

As per claim 19:

A first control device receiving task commands corresponding to respective active memory operations (Claim 1 line 1 "An integrated active memory device comprising" and lines 16 - 20), the first control device being operable to generate either

a respective set of memory commands or a respective set of processing commands responsive to each of the task commands (Claim 1 lines 16 - 20);

a second control device coupled to receive the memory commands from the first control device, the second control device being operable to generate a respective set of the memory device instructions responsive to each of the memory commands (Claim 1 lines 11 - 15); and

a third control device coupled to receive the processing commands from the first control device, the third control device being operable to generate a respective set of the processing element instructions responsive to each of the processing commands (Claim 1 lines 8 – 10)

As per claim 32:

A host processor having a processor bus (Claim 19 line 1);

at least one input device coupled to the host processor through the processor bus (Claim 19 lines 2 - 3);

at least one output device coupled to the host processor through the processor bus (Claim 19 lines 5 - 6);

at least one data storage device coupled to the host processor through the processor bus (Claim 19 lines 7 - 8); and

an active memory device, comprising:

a memory device having a data bus containing a plurality of data bus bits (Claim 19 lines 10 - 11);

an array of processing elements with each processing element coupled to a respective group of the data bus bits, each of the processing elements having an instruction input coupled to receive processing element instructions for controlling the operation of the processing elements (Claim 19 lines 12 - 15);

an array control unit coupled to the processing elements in the array, the array control unit being operable to generate and to couple respective sets of the processing element instructions to the processing elements responsive to each of a plurality of array control unit commands applied to a command input of the array control unit (Claim 19 lines 16 - 18);

a memory device control unit coupled to the memory device, the memory device control unit being operable to generate and to couple respective sets of memory commands to the memory device responsive to each of a plurality of memory device control unit commands applied to a command input of the memory device control unit (Claim 19 lines 19 - 23); and

a command engine coupled to the array control unit and the memory device control unit, the command engine being operable to couple to the array control unit respective sets of the array control unit commands and to couple to the memory device control unit respective sets of the memory device control limit commands responsive to respective task commands applied to a task command input of the command engine from the host processor (Claim 19 lines 24 - 29).

As per claim 33:

The memory device comprises a dynamic random access memory device (Claim 33.)

As per claim 52:

Receiving a task command corresponding to an active memory operation (Claim 19 lines 28 – 29 The preamble makes clear the invention is intended for memory commands received from the host processor as demonstrated in figure 1);

Responsive to the task command, generating either a set of array commands or a set of memory device commands (Claim 19 lines 26 – 27 "...couple to the array control unit respective sets of the array control unit commands..." and lines 27 – 28 "...couple to the memory device control unit respective sets of the memory device control unit commands...");

Responsive to each of the array commands, generating a respective set of processing element instructions (Claim 19 lines 16 – 18);

Responsive to each of the memory device commands, generating a respective set of memory device instructions (Claim 19 lines 20 - 21);

Coupling the processing element instructions to the processing elements and

Coupling the memory device instructions to the memory device. (Claim 19 lines 26 – 27 "...couple to the array control unit respective sets of the array control unit commands..." and lines 27 – 28 "...couple to the memory device control unit respective sets of the memory device control unit commands...");

5. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 19 is rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pre-Grant Publication 2003/0,097,389 (Saulsbury et al.)

As per claim 19, Saulsbury teaches:

A first control device receiving task commands corresponding to respective active memory operations, the first control device being operable to generate either a respective set of memory commands or a respective set of processing commands responsive to each of the task commands (Saulsbury ¶22 lines 1 – 6);

A second control device coupled to receive the memory commands from the first control device, the second control device being operable to generate a respective set of the memory device instructions responsive to each of the memory commands (Saulsbury ¶24 lines 2 - 5); and

A third control device coupled to receive the processing commands from the first control device, the third control device being operable to generate a respective set of

the processing element instructions responsive to each of the processing commands (Saulsbury ¶22 lines 6 - 10)

Allowable Subject Matter

8. Claims 3 - 18, 20 – 31, 34 - 51, and 53 - 65 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kaushikkumar Patel
Examiner
Art Unit 2188

kmp

3/31/06